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| **ram Project Status (09/09/2025 - 03:17:24)** | | | |
| **Project File:** | ram.xise | **Parser Errors:** | No Errors |
| **Module Name:** | ram | **Implementation State:** | Programming File Generated |
| **Target Device:** | xc3s400-4ft256 | * **Errors:** | No Errors |
| **Product Version:** | ISE 14.6 | * **Warnings:** | [7 Warnings (7 new)](D://ms/ram/_xmsgs/*.xmsgs?&DataKey=Warning) |
| **Design Goal:** | Balanced | * **Routing Results:** | [All Signals Completely Routed](D://ms/ram/ram.unroutes) |
| **Design Strategy:** | [Xilinx Default (unlocked)](Xilinx%20Default%20(unlocked)?&DataKey=Strategy) | * **Timing Constraints:** | [All Constraints Met](D://ms/ram/ram.ptwx?&DataKey=ConstraintsData) |
| **Environment:** | [System Settings](D://ms/ram/ram_envsettings.html) | * **Final Timing Score:** | 0  [(Timing Report)](D://ms/ram/ram.twx?&DataKey=XmlTimingReport) |

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| **Device Utilization Summary** | | | | | [**[-]**](?&ExpandedTable=DeviceUtilizationSummary) |
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Flip Flops | 26 | 7,168 | 1% |  | |
| Number of 4 input LUTs | 1 | 7,168 | 1% |  | |
| Number of occupied Slices | 13 | 3,584 | 1% |  | |
| Number of Slices containing only related logic | 13 | 13 | 100% |  | |
| Number of Slices containing unrelated logic | 0 | 13 | 0% |  | |
| Total Number of 4 input LUTs | 26 | 7,168 | 1% |  | |
| Number used as logic | 1 |  |  |  | |
| Number used as a route-thru | 25 |  |  |  | |
| Number of bonded [IOBs](D://ms/ram/ram_map.xrpt?&DataKey=IOBProperties) | 26 | 173 | 15% |  | |
| Number of RAMB16s | 1 | 16 | 6% |  | |
| Number of BUFGMUXs | 1 | 8 | 12% |  | |
| Average Fanout of Non-Clock Nets | 1.00 |  |  |  | |

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| **Performance Summary** | | | | [**[-]**](?&ExpandedTable=PerformanceSummary) |
| **Final Timing Score:** | 0 (Setup: 0, Hold: 0) | **Pinout Data:** | [Pinout Report](D://ms/ram/ram_par.xrpt?&DataKey=PinoutData) | |
| **Routing Results:** | [All Signals Completely Routed](D://ms/ram/ram.unroutes) | **Clock Data:** | [Clock Report](D://ms/ram/ram_par.xrpt?&DataKey=ClocksData) | |
| **Timing Constraints:** | [All Constraints Met](D://ms/ram/ram.ptwx?&DataKey=ConstraintsData) |  |  | |

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| **Detailed Reports** | | | | | | [**[-]**](?&ExpandedTable=DetailedReports) |
| **Report Name** | **Status** | **Generated** | **Errors** | **Warnings** | **Infos** | |
| [Synthesis Report](D://ms/ram/ram.syr) | Current | Tue 9. Sep 03:09:43 2025 | 0 | [3 Warnings (3 new)](D://ms/ram/_xmsgs/xst.xmsgs?&DataKey=Warning) | [2 Infos (2 new)](D://ms/ram/_xmsgs/xst.xmsgs?&DataKey=Info) | |
| [Translation Report](D://ms/ram/ram.bld) | Current | Tue 9. Sep 03:17:08 2025 | 0 | 0 | 0 | |
| [Map Report](D://ms/ram/ram_map.mrp) | Current | Tue 9. Sep 03:17:12 2025 | 0 | 0 | [2 Infos (2 new)](D://ms/ram/_xmsgs/map.xmsgs?&DataKey=Info) | |
| [Place and Route Report](D://ms/ram/ram.par) | Current | Tue 9. Sep 03:17:16 2025 | 0 | [4 Warnings (4 new)](D://ms/ram/_xmsgs/par.xmsgs?&DataKey=Warning) | [3 Infos (3 new)](D://ms/ram/_xmsgs/par.xmsgs?&DataKey=Info) | |
| Power Report |  |  |  |  |  | |
| [Post-PAR Static Timing Report](D://ms/ram/ram.twr) | Current | Tue 9. Sep 03:17:19 2025 | 0 | 0 | [6 Infos (6 new)](D://ms/ram/_xmsgs/trce.xmsgs?&DataKey=Info) | |
| [Bitgen Report](D://ms/ram/ram.bgn) | Current | Tue 9. Sep 03:17:23 2025 | 0 | 0 | [1 Info (1 new)](D://ms/ram/_xmsgs/bitgen.xmsgs?&DataKey=Info) | |

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| **Secondary Reports** | | | [**[-]**](?&ExpandedTable=SecondaryReports) |
| **Report Name** | **Status** | **Generated** | |
| [WebTalk Report](D://ms/ram/usage_statistics_webtalk.html) | Current | Tue 9. Sep 03:17:23 2025 | |
| [WebTalk Log File](D://ms/ram/webtalk.log) | Current | Tue 9. Sep 03:17:24 2025 | |

**Date Generated:** 09/09/2025 - 03:17:24